WHAT IS CLAIMED IS:

1. A method for initializing a memory circuit comprising:

detecting that a power supply operably coupled to the memory circuit first achieves a first predetermined voltage; and

asynchronously pulsing successive word line groups of one or more individual word lines of the memory array while conveying a data pattern onto bit lines of the memory array, to thereby write the data pattern into memory cells associated with each such word line group.

2. The method, as recited in claim 1, wherein each word line group pulse is non-overlapping with other such word line group pulses.

3. The method, as recited in claim 1, wherein word line groups include a single individual word line.

4. The method, as recited in claim 1, wherein word line groups include more than one individual word line.

5. The method, as recited in claim 4, wherein word lines within a group are physically adjacent word lines.

6. The method, as recited in claim 1, wherein the asynchronously pulsing includes, for at least one word line group:

pulsing a first word line group in response to an input signal received from an earlier pulsed second word line group;

generating an output signal delayed from the input signal; and

conveying the delayed output signal to a third word line group.

7. The method, as recited in claim 1, wherein each word line group is driven by a respective driver circuit, at least one driver circuit being enabled in response to a signal received from a driver circuit for a previously enabled word line group, and wherein at least one driver circuit generates a delayed output signal for enabling another word line group.

8. The method, as recited in claim 1, further comprising:
ensuring at least one data latch powers up having a first predetermined state corresponding to at least one bit of the data pattern.

9. The method, as recited in claim 1, further comprising:
ensuring a write enable latch node powers up having a state for enabling bit line drivers to the memory circuit.

10. The method, as recited in claim 1, wherein the memory circuit is initialized within a maximum of one clock cycle.

11. The method, as recited in claim 1, further comprising:
effectively disabling initialization circuitry after initializing the memory circuit.

12. The method, as recited in claim 1, wherein a node responsive to an input/output signal indicates that the power supply node achieved the first predetermined voltage.

13. The method, as recited in claim 1, wherein a circuit coupled to a power supply node indicates that the power supply achieved the first predetermined voltage.

14. The method, as recited in claim 13, wherein the circuit continues to indicate that the power supply node achieved the first predetermined voltage while the power supply node conveys a voltage greater than a second predetermined voltage less than the first predetermined voltage.

15. The method, as recited in claim 1, further comprising:
selectively configuring the data pattern.

16. A system comprising:
an array of memory cells arranged in rows and columns;
a plurality of word lines corresponding to respective rows of the array;
a plurality of bit lines corresponding to respective columns of the array;

a plurality of serially-connected word line driver initialization circuits, each for pulsing a respective group of one or more individual word lines of the memory array;

a control circuit for generating an input signal for the first of the serially-connected word line driver initialization circuits when a power supply operably coupled to the memory circuit first achieves a first predetermined voltage; and

a plurality of data circuits for conveying a data pattern onto the bit lines of the memory array during the pulsing of the word line groups.

17. The system, as recited in claim 16, wherein at least one word line driver is responsive to a respective input signal received from another word line driver initialization circuit and generating a respective output signal delayed from its respective input signal and conveying said delayed output signal to yet another word line driver initialization circuit.

18. The system, as recited in claim 16, wherein each word line driver initialization circuit respectively comprises:

a control input for receiving a control signal;

an output for conveying a word line pulse reset; and

an output for conveying a word line pulse based at least in part on the control signal and the word line pulse reset.

19. The system, as recited in claim 16, wherein the plurality of data circuits are coupled to power up having the data pattern.

20. The system, as recited in claim 16, wherein the input signal is based at least in part on a signal received from an input/output pin.

21. The system, as recited in claim 16, wherein the input signal is based at least in part on a first signal generated by an initialization circuit.

22. The system, as recited in claim 21, further comprising:

the initialization circuit including a first circuit, the first circuit being coupled to a first node and the power supply, the first circuit generating an enable signal having a response based at least in part on the power supply and the first predetermined voltage.

23. The system, as recited in claim 22, wherein the initialization circuit includes a second circuit responsive to the enable signal and having a first switching threshold level for a rising enable signal and a second switching threshold for a falling enable signal.

24. The system, as recited in claim 22, wherein the plurality of driver circuits are effectively disabled after initializing the memory array and while the power supply effectively maintains a voltage greater than a second predetermined voltage.

25. The system, as recited in claim 16, further comprising:

a plurality of delay elements corresponding to respective ones of the plurality of word line driver initialization circuits.

26. An integrated circuit comprising:

a first node, the first node conveying an enable signal;

a second node, the second node conveying an initialization signal;

a level shifting circuit coupled to the first node and a power supply node, the level shifting circuit generating the enable signal based at least in part on a signal conveyed by the power supply node and a predetermined initialization disable voltage;

a hysteresis circuit coupled to the first and second nodes, the hysteresis circuit generating the initialization signal; and

a latch node coupled to receive a first predetermined state in response to a first signal based at least in part on the initialization signal.

27. The integrated circuit, as recited in claim 26, wherein the latch node is coupled to power up having a predetermined state.

28. The integrated circuit, as recited in claim 26, wherein the latch node is coupled to receive data after the latch node is initialized.

29. The integrated circuit, as recited in claim 26, wherein the level shifting circuit includes a variable number of level shifting stages.

30. The integrated circuit, as recited in claim 34, wherein each level shifting stage includes a series device coupled to a load device.

31. The integrated circuit, as recited in claim 35, wherein the series device is a p-type transistor having a gate coupled to a ground node.

32. The integrated circuit, as recited in claim 35, wherein the load device is a weak n-type transistor having a gate coupled to a power supply node.

33. The integrated circuit, as recited in claim 26, further comprising:
a first selectable connector coupled to the latch node.

34. The integrated circuit, as recited in claim 33, wherein the latch node is selectably coupled to receive the predetermined state in response to the first signal based at least in part on the initialization signal.

35. The integrated circuit, as recited in claim 26, further comprising:
a weak device coupled to the second node.

36. The integrated circuit, as recited in claim 35, wherein the weak device is coupled to prevent the second node from discharging.

37. The integrated circuit, as recited in claim 26, wherein the second circuit has a first switching threshold level for a rising enable signal and a second switching threshold for a falling enable signal.

38. The integrated circuit, as recited in claim 37, wherein the second circuit is a Schmitt trigger circuit.

39. The integrated circuit, as recited in claim 26, further comprising:
a circuit responsive to a first pulse based at least in part on the initialization signal, and coupled to select at least one row of memory cells during a first interval.

40. The integrated circuit, as recited in claim 39, further comprising:
an additional circuit responsive to a second pulse and coupled to select an additional row of memory cells during a second interval.

41. The integrated circuit, as recited in claim 40, further comprising:
wherein the second pulse is later than the first pulse.

42. The integrated circuit, as recited in claim 26, further comprising:
a write enable node coupled to receive a second predetermined state in response to a signal based at least in part on the initialization signal, where in the second predetermined state enables writes to the memory circuit.

43. The integrated circuit, as recited in claim 26, embodied in computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit.

44. An apparatus comprising:
means for detecting that a power supply operably coupled to the memory circuit first achieves a first predetermined voltage; and
means for asynchronously pulsing successive word line groups of one or more individual word lines of the memory array while conveying a data pattern onto bit lines of the memory array, to thereby write the data pattern into memory cells associated with each such word line group.

45. The apparatus, as recited in claim 44, further comprising:
means for pulsing a first word line group in response to an input signal received from an earlier pulsed second word line group;
means for generating an output signal delayed from the input signal; and

means for conveying the delayed output signal to a third word line group.

46. The apparatus, as recited in claim 44, further comprising:
means for ensuring at least one data latch powers up having a first predetermined state corresponding to at least one bit of the data pattern.

47. The apparatus, as recited in claim 44, further comprising:
means for ensuring a write enable latch node powers up having a state for enabling bit line drivers to the memory circuit.

48. The apparatus, as recited in claim 44, further comprising:
means for effectively disabling initialization circuitry after initializing the memory circuit.

49. The apparatus, as recited in claim 44, further comprising:
means for selectively configuring the data pattern.